

JEDEC STANDARD

Definition of the SSTV32852 2.5-V 24-Bit to 48-Bit SSTL_2 Registered Buffer for 1U Stacked DDR DIMM Applications

JESD82-6A.01

(Editorial revision of JESD82-6A, November 2004)

JANUARY 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2023
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE

THE LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

This page intentionally left blank

STANDARD FOR DEFINITION OF THE SSTV32852 2.5-V AND SSTVA32852 2.6-V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFERS FOR STACKED DDR DIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-68, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the 32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications.

The purpose is to provide a standard for the 32852 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation 32852 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 24-bit to 48-bit registered buffer specification covers two speed grades; the faster speed grade SSTVA is backward compatible with the slower speed grade SSTV. These devices are collectively referred to as “32852” when it applies to both speed grades. These devices are intended to support the following applications:

Table 1 — 32852 Devices

Application	VDD/VDDQ Supply Voltage	32852 Part Number
PC1600 PC2100 PC2700	2.5 V \pm 0.2 V	SSTV32852 or SSTVA32852
PC3200	2.6 V \pm 0.1 V	SSTVA32852

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The 32852 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR DIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and

2 Device Standard (cont'd)

$\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain low.

Package options include 114 pin Low-Profile Fine Pitch BGA (LFBGA) (19 x 6 array, 16.00 x 5.50 mm body size, 0.80 mm pitch, MO-205, Variation DC).

2.2 Pinout Figure

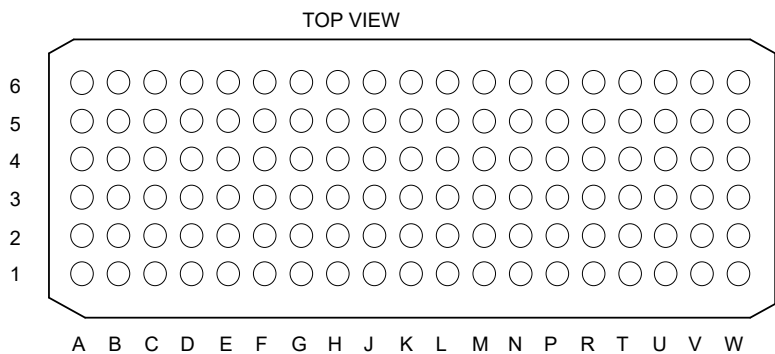


Figure 1 — 114-ball BGA Package Top View

6	Q2B	Q3B	Q5B	Q7B	Q8B	Q10B	Q12B	Q13B	Q14B	Q17B	Q18B	Q20B	Q22B	Q23B	Q24B	D14	D16	D17	D20
5	Q1B	V _{DDQ}	Q4B	Q6B	GND	Q9B	Q11B	V _{DD}	Q15B	Q16B	Q19B	V _{DDQ}	Q21B	V _{DDQ}	V _{DD}	D13	D15	D19	D21
4	$\overline{\text{CK}}$	GND	V _{DDQ}	GND	V _{DDQ}	V _{DDQ}	GND	V _{DDQ}	GND	V _{DDQ}	GND	GND	V _{DDQ}	GND	V _{REF}	D18	D22	D23	D24
3	CK	GND	V _{DDQ}	GND	V _{DDQ}	V _{DDQ}	GND	V _{DDQ}	GND	V _{DDQ}	GND	GND	V _{DDQ}	GND	RESET	D6	D10	D11	D12
2	Q1A	V _{DDQ}	Q4A	Q6A	GND	Q9A	Q11A	V _{DD}	Q15A	Q16A	Q19A	V _{DDQ}	Q21A	V _{DDQ}	V _{DD}	D1	D3	D7	D9
1	Q2A	Q3A	Q5A	Q7A	Q8A	Q10A	Q12A	Q13A	Q14A	Q17A	Q18A	Q20A	Q22A	Q23A	Q24A	D2	D4	D5	D8
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

Figure 2 — Pinout

2.3 Terminal Functions

Table 2 — Terminal Functions

Terminal name	Description	Electrical characteristics	
		SSTV	SSTVA
Q1–Q24	Data output	SSTL_2, Class II output	
GND	Ground	Ground input	
V _{DDQ}	Output-stage drain power voltage	2.5-V nominal	2.6-V nominal
V _{DD}	Logic power voltage	2.5-V nominal	2.6-V nominal
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables data and clock differential-input receivers	LVCMOS input	
V _{REF}	Input reference voltage	VDDQ / 2 nominal	
CK	Positive main clock input	Differential input	
$\overline{\text{CK}}$	Negative main clock input	Differential input	
D1–D24	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$	SSTL_2 input	

2.4 Function Table

Table 3 — Function Table (each Flip Flop)

Inputs				Q Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	D	
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	Q ₀
L	X or Floating	X or Floating	X or Floating	L

2.5 Logic Diagram

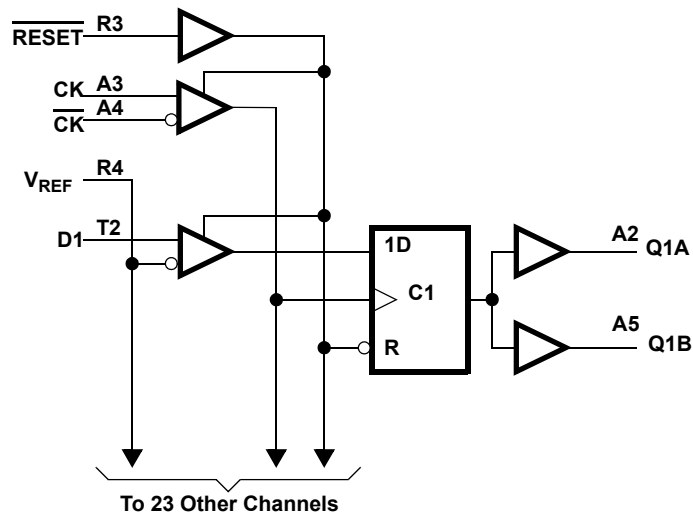


Figure 3 — Logic Diagram (Positive Logic)

2.6 Absolute Maximum Ratings

Table 4 — Absolute Maximum Ratings over Operating Free-air Temperature Range (see Note 1)

Supply voltage range, V_{DD} or V_{DDQ}	–0.5 V to 3.6 V
Input voltage range, V_I (See Notes 2 and 3)	–0.5 to $V_{DD} + 0.5$ V
Output voltage range, V_O (See Notes 2 and 3)	–0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	± 50 mA
Continuous current through each V_{DD} , V_{DDQ} or GND	± 100 mA
Storage temperature range, T_{STG}	–65 °C to 150 °C

- NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- NOTE 3 This value is limited to 3.6 V maximum.

2 Device Standard (cont'd)

2.7 Recommended Operating Conditions

Table 5 — Recommended Operating Conditions (see NOTE 1 and 2)

			Min	Nom	Max	Unit
V_{DD}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage		2.3		2.7	V
V_{REF}	Reference voltage		$(V_{DDQ} / 2) - 0.1$	$V_{DDQ} / 2$	$(V_{DDQ} / 2) + 0.1$	V
V_{TT}	Termination voltage		$V_{REF} - 40 \text{ mV}$	V_{REF}	$V_{REF} + 40 \text{ mV}$	V
V_I	Input voltage		0		V_{DD}	V
V_{IH}	AC high-level input voltage	Data inputs	$V_{REF} + 310 \text{ mV}$			V
V_{IL}	AC low-level input voltage	Data inputs			$V_{REF} - 310 \text{ mV}$	V
V_{IH}	DC high-level input voltage	Data inputs	$V_{REF} + 150 \text{ mV}$			V
V_{IL}	DC low-level input voltage	Data inputs			$V_{REF} - 150 \text{ mV}$	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input range	CK, \overline{CK}	0.97		1.53	V
V_{ID}	Differential input voltage	CK, \overline{CK}	360			mV
I_{OH}	High-level output current				-20	mA
I_{OL}	Low-level output current				20	
T_A	Operating free-air temperature		0		70	°C
NOTE 1	The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.					
NOTE 2	Supply voltages are shown for compatibility with SSTV and SSTVA applications. PC3200 applications require a $V_{DD} = V_{DDQ}$ of $2.6 \text{ V} \pm 0.1 \text{ V}$.					

2.8 DC Specifications

Table 6 — Electrical Characteristics over Recommended Operating Free-air Temperature Range

Parameter		Test conditions		V _{DD}	Min	Typ	Max	Unit
V _{IK}		I _I = -18 mA		2.3 V			-1.2	V
V _{OH}		I _{OH} = -100 μA		2.3 to 2.7 V	V _{DD} - 0.2			V
		I _{OH} = -16 mA		2.3 V	1.95			
V _{OL}		I _{OL} = 100 μA		2.3 to 2.7 V			0.2	V
		I _{OL} = 16 mA		2.3 V			0.35	
I _I	All inputs	V _I = V _{DD} or GND		2.7 V			±5	μA
I _{DD}	Static standby	$\overline{\text{RESET}}$ = GND		2.7 V			0.01	mA
	Static operating	$\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)}					†	
I _{DDD}	Dynamic operating – clock only	$\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK and $\overline{\text{CK}}$ switching 50% duty cycle		2.7 V			†	μA/ clock MHz
	Dynamic operating – per each data input	$\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK and $\overline{\text{CK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.					†	μA/ clock MHz/ data input
r _{OH}	Output high	I _{OH} = -20 mA		2.3 to 2.7 V	7		20	Ω
r _{OL}	Output low	I _{OL} = 20 mA		2.3 to 2.7 V	7		20	Ω
r _{O(Δ)}	r _{OH} - r _{OL} each separate bit	I _O = 20 mA, T _A = 25 °C		2.5 V			4	Ω
C _i	Data inputs	V _I = V _{REF} ± 310 mV		2.5 V	3		4.25	pF
	CK and $\overline{\text{CK}}$	V _{ICR} = 1.25 V, V _{I(PP)} = 360 mV			3		4	
	$\overline{\text{RESET}}$	V _I = V _{DD} or GND			†		†	

† The vendor must supply this value for full device description.

NOTE Supply voltages are shown for compatibility with SSTV and SSTVA applications. PC3200 applications require a VDD = VDDQ of 2.6 V ±0.1 V.

2 Device Standard (cont'd)

2.9 Timing Requirements

Table 7 — Timing Requirements over Recommended Operating Free-air Temperature Range

			min	max	Unit
f _{clock}	Clock frequency, SSTV		200		MHz
f _{clock}	Clock frequency, SSTVA		220		MHz
t _w	Pulse duration, CK, $\overline{\text{CK}}$ high or low, SSTV		2.5		ns
t _w	Pulse duration, CK, $\overline{\text{CK}}$ high or low, SSTVA		2.3		ns
t _{act} [†]	Differential inputs active time (see Note 1)		22		ns
t _{inact} [†]	Differential inputs inactive time (see Note 2)		22		ns
t _{su}	Setup time, fast slew rate (See Notes 3 and 5)	Data before CK ↑, $\overline{\text{CK}}$ ↓	0.75		ns
	Setup time, slow slew rate (See Notes 4 and 5)		0.9		
t _h	Hold time, fast slew rate (See Notes 3 and 5)	Data after CK ↑, $\overline{\text{CK}}$ ↓	0.75		ns
	Hold time, slow slew rate (See Notes 4 and 5)		0.9		

[†] This parameter is not necessarily production tested.

NOTE 1 Data inputs must be low a minimum time of t_{act} max, after $\overline{\text{RESET}}$ is taken high

NOTE 2 Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max, after $\overline{\text{RESET}}$ is taken low.

NOTE 3 For data signal input slew rate ≥ 1 V/ns.

NOTE 4 For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.

NOTE 5 CK, $\overline{\text{CK}}$ signals input slew rates are ≥ 1 V/ns.

2.10 AC Specifications

Table 8 — Switching Characteristics over Recommended Operating Free-air Temperature Range (unless otherwise noted) (see Figure 3)

Parameter	From (Input)	To (Output)	SSTV		SSTVA		Unit
			Min	Max	Min	Max	
f_{max}			200		220		MHz
t_{pd}	CK and $\overline{\text{CK}}$	Q	1.1	3.1	1.1	2.0	ns
t_{PHL}	$\overline{\text{RESET}}$	Q		5		5	ns

3 Output Buffer Characteristics

3.1 Voltage vs. Current (V/I)

The following table describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these curves is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application.

Table 9 — Output Buffer Voltage vs. Current (V/I) Characteristics

Voltage (V)	Pull-down		Pull-Up	
	I(mA)	I(mA)	I(mA)	I(mA)
	MIN	MAX	MIN	MAX
0	0	0	0	-0
0.1	5	18	-5	-18
0.2	10	30	-10	-30
0.3	15	44	-15	-44
0.4	19	55	-19	-55
0.5	23	67	-23	-67
0.6	27	78	-27	-78
0.7	30	90	-30	-90
0.8	34	101	-34	-98
0.9	36	112	-36	-106
1.0	38	121	-38	-113
1.1	40	131	-40	-119
1.2	42	140	-42	-125
1.3	43	150	-43	-130
1.4	44	159	-44	-134
1.5	44	167	-44	-137
1.6	45	176	-45	-140
1.7	45	184	-45	-143
1.8	45	192	-45	-146
1.9	45	199	-45	-149
2.0	45	206	-45	-152
2.1	46	212	-46	-154
2.2	46	218	-46	-156
2.3	46	222	-46	-157
2.4	46	226	-46	-159
2.5	46	229	-46	-160
2.6	46	233	-46	-161
2.7	46	234	-46	-162

3 Output Buffer Characteristics (cont'd)

3.2 Slew Rate

The following table describes output-buffer slew-rate characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these rates is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application. This information does not necessarily have to appear in the device datasheet.

Obtain rise and fall time measurements by using the same procedure for obtaining “[Ramp]” data according to the current EIA IBIS specification. In particular it is very important to note that the following slew rates are specified at the output of the die, **without** package parasitics in the power, ground or output paths. The measurement points are at 20% and 80%. The slew-rate test load shall be a 50 Ω resistor to GND for Rise, and a 50 Ω resistor to V_{DDQ} for Fall. The dV/dt ratio is reduced to V/ns.

Table 10 — Output-buffer Slew Rate Characteristics

dV/dt	Min	Max
Rise	1.1 V/ns	13.9V/ns
Fall	1.1 V/ns	14.5 V/ns

3.3 Simultaneous Switching

The vendor must supply, as requested, simultaneous switching information for full device description. In particular, slow corner propagation-delay increase due to simultaneous switching conditions is necessary for post-register timing analysis. This information does not necessarily have to appear in the device datasheet.

4 Test Circuit and Switching Waveforms

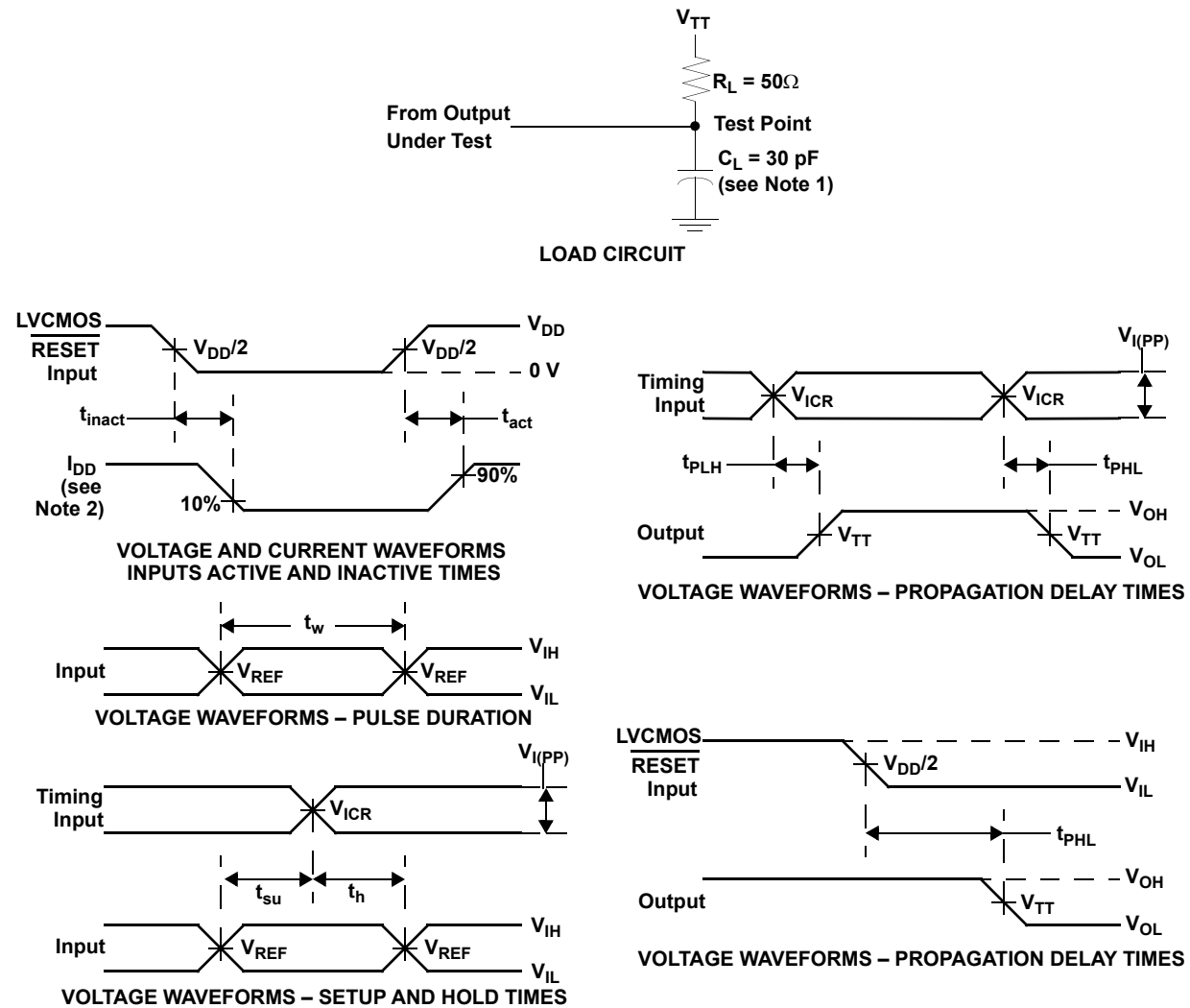


Figure 4 — Parameter Measurement Information ($V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$)

NOTE 1 C_L includes probe and jig capacitance.

NOTE 2 I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0 \text{ mA}$.

NOTE 3 All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise specified).

NOTE 4 The outputs are measured one at a time with one transition per measurement.

NOTE 5 $V_{TT} = V_{REF} = V_{DDQ}/2$

NOTE 6 $V_{IH} = V_{REF} + 310 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS input.

NOTE 7 $V_{IL} = V_{REF} - 310 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.

NOTE 8 t_{PLH} and t_{PHL} are the same as t_{pd}

5 Reference to Other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*
- JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices*
- JESD8-5, *2.5 Volt ± 0.2 V (Normal Range) and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface for Non-terminated Digital Integrated Circuits.*
- JESD8-9, *Stub Series Terminated Logic for 2.5 V (SSTL_2)*
- JESD21-C, *Configuration for Solid State Memories*

Annex A — (Informative) Differences between JESD82-6A and JESD82-6

This table briefly describes most of the changes made to entries that appear in this standard, JESD82-6A, compared to its predecessor, JESD82-6 (November 2002). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page Description of change

New	Old	Change text
1	1	Inserted: “and SSTVA32852 2.6...”
1	1	Replaced: “SSTL_2 ” With: “SSTL_2 ”c
1	1	Replaced: “BUFFER ” With: “BUFFERS ”
1	1	Replaced: “02” With: “04”
1	1	Replaced: “87” With: “68”
1	1	Replaced: “.)” With: “. ”
1	1	Replaced: “SSTV32852 ” With: “32852 ”
1	1	Replaced: “SSTV32852 ” With: “32852 ”
1	1	Replaced: “SSTV32852 ” With: “32852 ”
1	1	Replaced: “This 24-bit to ...” With: “This 24-bit to ...”
1	1	Replaced: “SSTV32852 ” With: “32852 ”
1	1	Inserted: “In the DDR DIMM application...”
1	1	Deleted: “In the DDR DIMM application...”
2	2	Deleted: “2 Device standard (...”
4	4	Deleted: “2 Device standard (...”
5	4	Inserted: “2 Device standard (...”
5	4	Replaced: “voltage (VREF = VDDQ ...” With: “voltage”
5	4	Replaced: “1.15” With: “(VDDQ / 2) ...”
5	4	Replaced: “1.25” With: “VDDQ / 2”
5	4	Replaced: “1.35” With: “(VDDQ / 2) ...”
5	4	Inserted: “Supply voltages are shown for ...”
6	5	Inserted: “Supply voltages are shown for ...”
12	10	Inserted: “Annex A (informative) ...”

Table Changes

New	Old	Change Table Title
1	1	Inserted 3: 2852 Devices
3	2	Changed: Terminal functions
7	6	Changed: Timing requirements over recommended operating...
7	6	Changed: Switching characteristics over recommended operating ...

Annex B — (Informative) Differences between JESD82-6A.01 and JESD82-6A

Editorial changes as follows:

- Clause 2.3, Table 2: changed “master” to “main” for the definition of CK and $\overline{\text{CK}}$
- Updated JEDEC logos and back pages to standard format
- All headings, figure titles, and table titles changed to Initial Caps



Standard Improvement Form**JEDEC Standard JESD82-6A.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC

Attn: Publications Department
3103 North 10th Street, Suite 240S
Arlington, VA 22201-2107
Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

Name: _____

Company: _____

Address: _____

City/State/Zip: _____

Phone: _____

E-mail: _____

Date: _____

